

AMENDMENTS TO THE CLAIMS

Claims 1-7 (Cancelled)

8. (Currently Amended) A method of forming a semiconductor device, the method comprising:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a first opening that defines a first side wall and an opposing second side wall;

forming a first layer of conductive material on the layer of insulation material to contact the first opening;

etching the first layer of conductive material to form a first conductive spacer that adjoins the first side wall and the second side wall, and a second opening;

forming a first layer of isolation material on the layer of insulation material and the first conductive spacer to contact the second opening;

~~forming a conductive region on the first conductive spacer and the first layer of isolation material, the conductive region making an electrical connection with the first conductive spacer;~~

etching the first layer of isolation material to form a first isolation spacer that adjoins the first conductive spacer, and a third opening;

forming a second layer of conductive material on the layer of insulation material to contact the third opening;

etching the second layer of conductive material to form a second conductive spacer that adjoins the first isolation spacer, and a fourth opening; ~~and~~

forming a second layer of isolation material on the layer of insulation material and the second conductive spacer to contact the fourth opening, and

forming a conductive region on the first conductive spacer and the first layer of isolation material, the conductive region contacting the first and second conductive spacers to make an electrical connection.

9. (Currently Amended) ~~The method of claim 7 and further comprising~~
A method of forming a semiconductor device, the method comprising:

forming a layer of insulation material over a semiconductor substrate;

removing a region of the layer of insulation material that has a length, a width, and a depth to define a first opening in the layer of insulation material that has the length, the width, and the depth, the first opening having a first side wall and an opposing second side wall;

forming a layer of conductive material on the layer of insulation material and in the first opening;

etching the layer of conductive material to form a conductive spacer that contacts the first side wall and the second side wall, and a second opening that contacts a side wall of the conductive spacer;

forming a layer of isolation material in the second opening and to contact the layer of insulation material and the conductive spacer; and

planarizing the layer of insulation material, the conductive spacer, and the layer of isolation material until the layer of insulation material, the conductive spacer, and the layer of isolation material have a substantially planar top surface.

10. (Previously Presented) The method of claim 8 and further comprising planarizing the layer of insulation material, the first conductive spacer, the first layer of isolation material, the second conductive spacer, and the second layer of isolation material until the layer of insulation material, the first conductive spacer, the first layer of isolation material, the second conductive spacer, and the second layer of isolation material have a substantially planar top surface.

11. (Currently Amended) ~~The method of claim 7 and further comprising:~~ A method of forming a semiconductor device, the method comprising:
forming a layer of insulation material over a semiconductor substrate;
removing a region of the layer of insulation material that has a length, a width, and a depth to define a first opening in the layer of insulation material that has the length, the width, and the depth, the first opening having a first side wall and an opposing second side wall;
forming a layer of conductive material on the layer of insulation material and in the first opening;
etching the layer of conductive material to form a conductive spacer that contacts the first side wall and the second side wall, and a second opening that contacts a side wall of the conductive spacer;
forming a layer of isolation material in the second opening and to contact the layer of insulation material and the conductive spacer;
etching the layer of isolation material to form an isolation spacer that contacts the side wall of the conductive spacer, and a hole that contacts a side wall of the isolation spacer; and

forming a layer of conducting material in the hole and to contact the layer of insulation material and the conductive spacer.

12. (Previously Presented) The method of claim 8 wherein forming a conductive region includes:

forming a third layer of conductive material on the layer of insulation material, the first conductive spacer, the first layer of isolation material, and the second conductive spacer;

forming a mask on the third layer of conductive material that exposes regions of the third layer of conductive material; and

etching the exposed regions of the third layer of conductive material.

13. (Currently Amended) ~~The method of claim 7 wherein the first opening is formed to have~~ A method of forming a semiconductor device, the method comprising:

forming a layer of insulation material over a semiconductor substrate;

removing a region of the layer of insulation material that has a length, a width, and a depth to define a first opening in the layer of insulation material that has the length, the width, and the depth, the first opening having a first side wall, an opposing second side wall, and a number of loops;

forming a layer of conductive material on the layer of insulation material and in the first opening;

etching the layer of conductive material to form a conductive spacer that contacts the first side wall and the second side wall, and a second opening that contacts a side wall of the conductive spacer;

forming a layer of isolation material in the second opening and to contact the layer of insulation material and the conductive spacer.

Claims 14-17 (Cancelled)

18. (Currently Amended) ~~The method of claim 17 and further comprising:~~ A method of forming a semiconductor device on an insulation region, the insulation region having a top surface, the method comprising:

forming a trench in the insulation region, the trench having a side wall surface and a bottom surface, the side wall surface extending continuously from the top surface to the bottom surface, the side wall surface exposing only the insulation region, a portion of the bottom surface of the trench exposing a region of a conductive material;

forming a layer of conductive material on the insulation region to contact the top surface of the insulation region, the side wall surface of the trench, and the bottom surface of the trench;

etching the layer of conductive material to form a conductive spacer that contacts the side wall surface, and an opening that contacts a side wall of the conductive spacer;

forming a layer of isolation material in the opening and to contact the insulation region and the conductive spacer;

etching the layer of isolation material to expose the conductive spacer; and
forming a conductor on the conductive spacer and the layer of isolation material, the conductor making an electrical connection with the conductive spacer.

19. (Currently Amended) ~~The method of claim 17 and further comprising:~~ A method of forming a semiconductor device on an insulation region, the insulation region having a top surface, the method comprising:

forming a trench in the insulation region, the trench having a side wall surface and a bottom surface, the side wall surface extending continuously from the top surface to the bottom surface, the side wall surface exposing only the insulation region, a portion of the bottom surface of the trench exposing a region of a conductive material;

forming a layer of conductive material on the insulation region to contact the top surface of the insulation region, the side wall surface of the trench, and the bottom surface of the trench;

etching the layer of conductive material to form a conductive spacer that contacts the side wall surface, and an opening that contacts a side wall of the conductive spacer;

forming a layer of isolation material in the opening and to contact the insulation region and the conductive spacer;

etching the layer of isolation material to form an isolation spacer that contacts the side wall of the conductive spacer, and a hole that contacts a side wall of the isolation spacer; and

forming a layer of conducting material in the hole and to contact the insulation region and the conductive spacer.

20. (Cancelled)

21. (Previously Presented) The method of claim 19 and further comprising:

etching the layer of conducting material to remove the layer of conducting material from the top surface of the insulation region, and form an interior spacer that contacts the side wall of the isolation spacer, and an aperture that contacts a side wall of the interior spacer, the interior spacer being conductive; and

forming a layer of insulation material in the aperture and to contact the insulation region, the conductive spacer, and the isolation spacer.

22. (Previously Presented) The method of claim 21 and further comprising:

etching the layer of insulation material to remove the layer of insulation material from the top surface of the insulation region, a top surface of the conductive spacer, and a top surface of the interior spacer; and

forming a conductor on the conductive spacer, the isolation spacer, the interior spacer, and the layer of insulation material in the aperture, the conductor contacting the conductive spacer and the interior spacer to make an electrical connection.

23. (Currently Amended) ~~The method of claim 17 and further comprising:~~ A method of forming a semiconductor device on an insulation region, the insulation region having a top surface, the method comprising:

forming a trench in the insulation region, the trench having a side wall surface and a bottom surface, the side wall surface extending continuously from the top surface to the bottom surface, the side wall surface exposing only the insulation

region, a portion of the bottom surface of the trench exposing a region of a conductive material;

forming a layer of conductive material on the insulation region to contact the top surface of the insulation region, the side wall surface of the trench, and the bottom surface of the trench;

etching the layer of conductive material to form a conductive spacer that contacts the side wall surface, and an opening that contacts a side wall of the conductive spacer;

forming a layer of isolation material in the opening and to contact the insulation region and the conductive spacer;

planarizing the insulation region, the conductive spacer, and the layer of isolation material until the insulation region, the conductive spacer, and the layer of isolation material have a substantially planar top surface; and

forming a conductor on the conductive spacer and the layer of isolation material, the conductor contacting the conductive spacer to make an electrical connection.

24. (Previously Presented) The method of claim 19 and further comprising:

planarizing the insulation region, the conductive spacer, the isolation spacer, and the layer of conducting material until the insulation region, the conductive spacer, the isolation spacer, and the layer of conducting material have a substantially planar top surface; and

forming a conductor on the conductive spacer, the isolation spacer, and the layer of conducting material, the conductor contacting the conductive spacer and the layer of conducting material to make an electrical connection.

25. (Previously Presented) The method of claim 18 wherein the trench is formed to have a number of loops.

26. (Previously Presented) The method of claim 18 wherein the opening exposes the bottom surface of the trench.

27. (Previously Presented) The method of claim 19 wherein the hole exposes the bottom surface of the trench.

28. (Cancelled)

29. (Currently Amended) ~~The method of claim 7 and further comprising:~~ A method of forming a semiconductor device, the method comprising:
forming a layer of insulation material over a semiconductor substrate;
removing a region of the layer of insulation material that has a length, a width,
and a depth to define a first opening in the layer of insulation material that has the
length, the width, and the depth, the first opening having a first side wall and an
opposing second side wall;
forming a layer of conductive material on the layer of insulation material and in
the first opening;

etching the layer of conductive material to form a conductive spacer that contacts the first side wall and the second side wall, and a second opening that contacts a side wall of the conductive spacer;

forming a layer of isolation material in the second opening and to contact the layer of insulation material and the conductive spacer;

etching the layer of isolation material to expose the conductive spacer; and
forming a conductor on the conductive spacer and the layer of isolation material, the conductor making an electrical connection with the conductive spacer.

30. (Previously Presented) The method of claim 11 and further comprising:

etching the layer of conducting material to remove the layer of conducting material from the top surface of the layer of insulation material, and form an interior spacer that contacts the side wall of the isolation spacer, and an aperture that contacts a side wall of the interior spacer, the interior spacer being conductive;

forming an insulating layer in the aperture and to contact the layer of insulation material, the conductive spacer, and the isolation spacer;

etching the insulating layer to remove the insulating layer from the top surface of the layer of insulation material, a top surface of the conductive spacer, and a top surface of the interior spacer; and

forming a conductor on the conductive spacer, the isolation spacer, the interior spacer, and the insulating layer in the aperture, the conductor contacting the conductive spacer and the interior spacer to make an electrical connection.